A 2W, 4 GHz GaAsFET AMPLIFIER FOR RADIO RELAY APPLICATIONS

W. E. Schroeder and J. W. Gewartowski
Bell Telephone Laboratories, Inc.
555 Union Boulevard
Allentown, PA, 18103

ABSTRACT

A 2W, 4 GHz GaAsFET amplifier has been developed with performance suitable for replacement of the close - spaced triode transmitter amplifier in the 4 GHz radio relay systems (TD-2 and TD-3D). The amplifier produces a minimum of 21dB of gain using three stages, with a single GaAsFET in each stage.

Introduction

GaAsFET devices have demonstrated greater than 15W of rf output power at 4 GHz. Their high gain, low noise, and low voltage operation make them an ideal device for microwave amplifier applications.

Some of the design objectives for a transmitter amplifier for 4 GHz microwave radio systems are:

1. 2W output power with 21dB gain.
2. Input and output return loss $\geq$ 25dB.
3. Flat gain ($\pm$ 0.10dB over a 20 MHz band is desirable).
4. Linearity consistent with digital transmission applications.
5. Harmonic output greater than 50dB below the carrier.
6. High reliability.
7. Low cost.

We have built and tested a number of models of an amplifier which meets these objectives. This paper describes the approach we have taken, the design of the FET matching networks to optimize the power output and linearity simultaneously, and typical performance data.

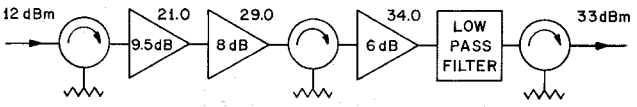

FIGURE 1: BLOCK DIAGRAM OF THE AMPLIFIER.

Arrangement of Components

A block diagram of the three-stage amplifier is shown in Figure 1, with the gain and output power of each stage indicated. It was decided to use a single transistor in each stage, rather than a balanced approach, to minimize the total transistor cost and improve the reliability. Input and output isolators are required to meet the match objectives. The low-pass filter is used to reduce 2nd and 3rd harmonic output power. The isolator between the second and third stages permits us to optimize the output power and linearity of the second stage FET and provides a convenient test point for independently tuning the two-stage preamplifier and the third stage.

The characteristics of the GaAsFET devices[1] are given in Table I. The power levels given on the block diagram show the allowances made for loss of the passive components. All stages are operated in the common source configuration.

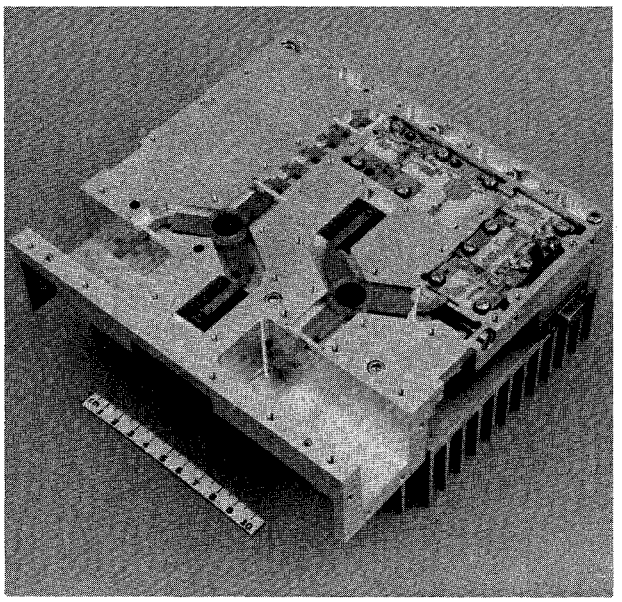

FIGURE 2: PHOTOGRAPH OF OPEN AMPLIFIER.

TABLE I

Stage	Gate Width mm	Drain Voltage V	Drain Current mA	Gain (Minimum) dB	Output Power @ Nominal Input Power Minimum dBm	Typical dBm
1	1	12	100	10.5	22	25
2	3	14	300	9.5	30	31
3	6	14	600-750	7.0	35	35.5

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Figure 2 is a photograph of the complete amplifier with the housing cover removed. The FETs are supplied in hermetically sealed, high-power packages of the bar type. They are fastened to copper carrier plates, to which the microstrip matching networks are soldered. There are two active microwave modules: the preamplifier, which contains the first two stages and the power amplifier, which contains a microstrip circulator and the third stage.

The input and output isolators and waveguide transducers are the same design as those used in a 4 GHz, low-noise amplifier[2]. The isolators are made in air-dielectric stripline. The center strip is stamped from brass sheet. The isolator terminations are wedges of commercially-available loss material and are designed to dissipate 5W CW. The low-pass filter is also realized in stripline. It is made from the same piece as the output isolator center strip. This stripline medium offers high performance components, with low-cost parts and assembly, and high yields.

Matching Network Design

Measurements of our transistors in a tunable test fixture have revealed that:

1. The load impedance for maximum output power is significantly different from the load impedance for maximum small-signal gain.
2. The source impedance for maximum output power is essentially the same as that for maximum small-signal gain.
3. The intermodulation distortion, IMD, at a fixed output power, as measured by a two-equal-tone test, is virtually independent of the source impedance but is dependent on the load impedance. Others have reported similar observations for GaAsFETs.[3,4]

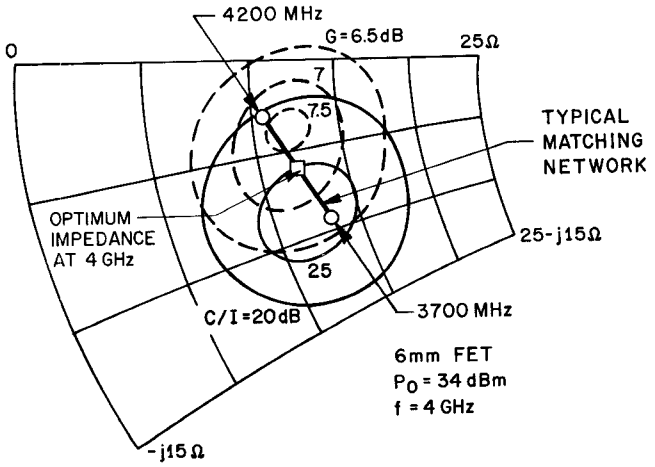

FIGURE 3: CONTOURS OF CONSTANT GAIN AND C/I IN THE LOAD IMPEDANCE PLANE FOR A THIRD STAGE GaAsFET.

Since the noise figure is not critical in our application, the source impedance is tuned for maximum output power. The load impedance for maximum output power is different from that for lowest IMD, so a compromise must be made. Figure 3 shows gain and C/I (ratio of the carrier to third-order intermodulation product with two equal input tones) as a function of load impedance, for a typical third-stage transistor. The data are measured in a load-pull test set at constant rf output power. The source impedance is tuned for maximum gain under small-signal conditions and kept fixed throughout the measurements.

To obtain the lowest IMD while maintaining reasonably high gain at the desired output power, the load impedance point shown in Figure 3 is chosen. We have used several different types of matching networks with satisfactory results: cascaded quarter-wavelength transformers, shunt open-circuit stubs, and series interdigital capacitors. Each of these is easily realized in microstrip. The impedance variation over the operating band is shown by the solid line in Figure 3 for a typical network.

The design of the matching networks for the 2-stage preamplifier is also based on the measured gain and IMD characteristics of the transistors. Since the preamplifier operates more linearly than the third stage, the small-signal s parameters of the FETs are a good performance guide. Computer analysis and optimization* of the matching networks has proved beneficial.

Performance

Although laboratory models of the complete amplifier were built having a minimum 21dB gain and 2W output power over the full common-carrier band of 3.7 to 4.2 GHz, it was decided to design for a bandwidth only half as large. This was considered to be acceptable for system applications, and it permitted optimized performance and greater ease of manufacture.

The output power versus frequency for an upper-half-band unit is shown in Figure 4. Output power versus input power is shown in Figure 5, at a frequency of 4.05 GHz. The power output at 1dB gain compression is 33.7dBm. Also plotted in Figure 5 is the two-equal-tone C/I ratio as a function of the total input power.

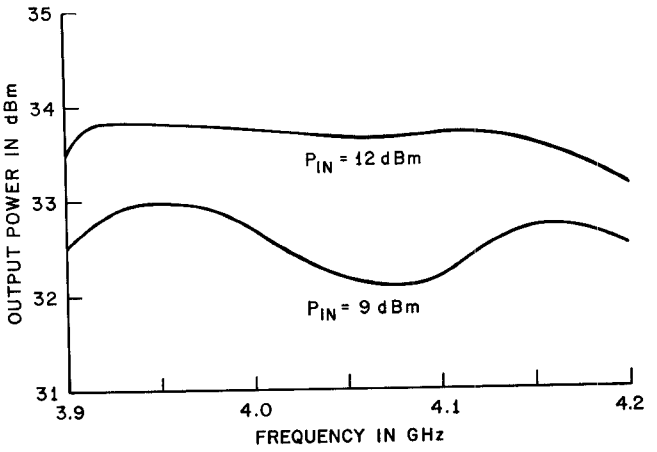

FIGURE 4: POWER VERSUS FREQUENCY FOR AN UPPER-HALF-BAND UNIT.

* COMPACT program, COMPACT Engineering, Inc.

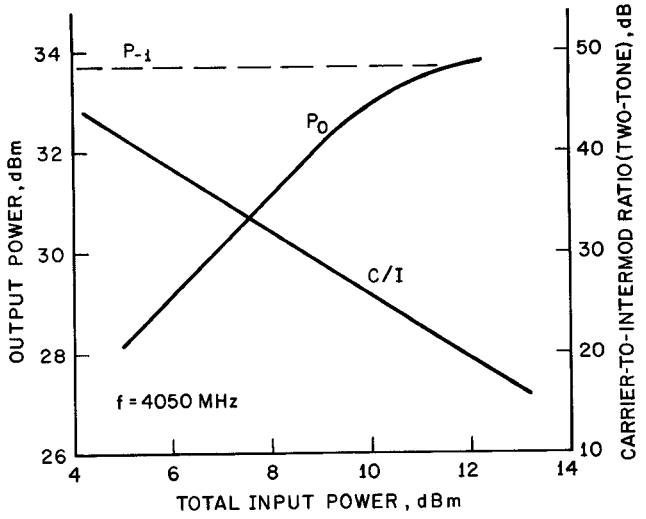

FIGURE 5: OUTPUT POWER AND C/I AS A FUNCTION OF THE INPUT POWER LEVEL.

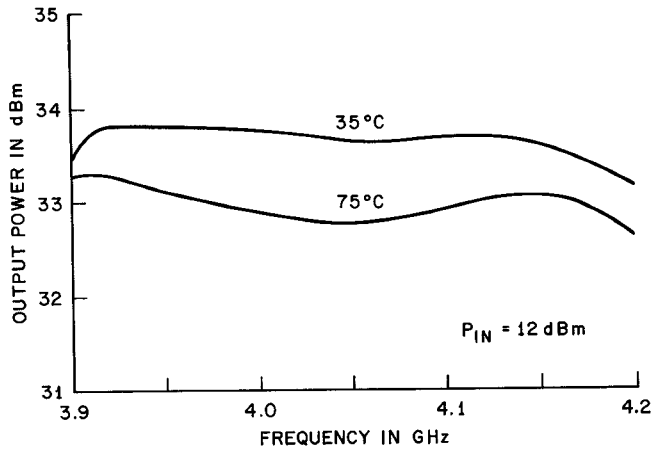

FIGURE 6: POWER VERSUS FREQUENCY AT TWO DIFFERENT HOUSING TEMPERATURES.

Figure 6 shows the variation of output power with housing temperature. The amplifier is cooled by free convection, and 35° C is the nominal operating temperature. The housing temperature of 75° C represents a worst-case value, showing a decrease of output power less than 1dB.

A field trial of the amplifier was held in the fourth quarter of 1977. The amplifier was found to be suitable both for FM and digital transmission.

Acknowledgments

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